Amendments to th Claims

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Claims 1-20 (Previously Canceled).

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21. (Currently Amended): DRAM circuitry comprising:

an array of word lines forming gates of field effect transistors and an array of bit lines, individual field effect transistors comprising a pair of source/drain regions; and

a plurality of memory cell storage capacitors associated with the field effect transistors, individual storage capacitors comprising a first capacitor electrode in electrical connection with one of a pair of source/drain regions of one of the field effect transistors and a second capacitor electrode, a capacitor dielectric region received intermediate the first and second capacitor electrodes, the region comprising dielectric aluminum nitride, the other of the pair of source/drain regions of the one field effect transistor being in electrical connection with one of the bit lines.

22. (Currently Amended): The circuitry of claim 21 wherein the region contacts each of the first and second capacitor electrodes and consists essentially of dielectric aluminum nitride.

23. (Currently Amended): The circuitry of claim 21 wherein the region contacts each of the first and second capacitor electrodes and consists essentially of dielectric aluminum nitride and native oxide formed on at least one of the first and second capacitor electrodes.

24. (Previously Amended): The circuitry of claim 21 wherein the region contacts each of the first and second capacitor electrodes and has a thickness less than or equal to 60 Angstroms.

25. (Previously Amended): The circuitry of claim 21 wherein the region contacts each of the first and second capacitor electrodes and has a thickness less than or equal to 50 Angstroms.

26. (Currently Amended): The circuitry of claim 21 wherein the region contacts each of the first and second capacitor electrodes, consists essentially of dielectric aluminum nitride, and has a thickness less than or equal to 60 Angstroms.

27. (Currently Amended): The circuitry of claim 21 wherein the region contacts each of the first and second capacitor electrodes, consists essentially of dielectric aluminum nitride and native oxide formed on at least one of the first and second capacitor electrodes, and has a thickness less than or equal to 60 Angstroms.

28. (Currently Amended): The circuitry of claim 21 wherein the dielectric aluminum nitride is substantially amorphous.

Claims 29-63 (Previously Canceled).

64. (Currently Amended): The circuitry of claim 28 wherein the region contacts each of the first and second capacitor electrodes and consists essentially of substantially amorphous dielectric aluminum nitride.

65. (Currently Amended): The circuitry of claim 28 wherein the region contacts each of the first and second capacitor electrodes and consists essentially of substantially amorphous dielectric aluminum nitride and native oxide formed on at least one of the first and second capacitor electrodes.

66. (Previously Added): The circuitry of claim 28 wherein the region contacts each of the first and second capacitor electrodes and has a thickness less than or equal to 60 Angstroms.

67. (Previously Added): The circuitry of claim 28 wherein the region contacts each of the first and second capacitor electrodes and has a thickness less than or equal to 50 Angstroms.

68. (Currently Amended): The circuitry of claim 28 wherein the region contacts each of the first and second capacitor electrodes, consists essentially of substantially amorphous dielectric aluminum nitride, and has a thickness less than or equal to 60 Angstroms.

69. (Currently Amended): The circuitry of claim 28 wherein the region contacts each of the first and second capacitor electrodes, consists essentially of substantially amorphous dielectric aluminum nitride and native oxide formed on at least one of the first and second capacitor electrodes, and has a thickness less than or equal to 60 Angstroms.

70. (Currently Amended): The circuitry of claim 28 wherein the region contacts each of the first and second capacitor electrodes, consists essentially of substantially amorphous dielectric aluminum nitride, and has a thickness less than or equal to 50 Angstroms.

71. (Currently Amended): The circuitry of claim 28 wherein the region contacts each of the first and second capacitor electrodes, consists essentially of substantially amorphous dielectric aluminum nitride and native oxide formed on at least one of the first and second capacitor electrodes, and has a thickness less than or equal to 50 Angstroms.

72. (Currently Amended): The circuitry of claim 21 wherein the region contacts each of the first and second capacitor electrodes, consists essentially of substantially amorphous dielectric aluminum nitride, and has a thickness less than or equal to 50 Angstroms.

73. (Currently Amended): The circuitry of claim 21 wherein the region contacts each of the first and second capacitor electrodes, consists essentially of substantially amorphous dielectric aluminum nitride and native oxide formed on at least one of the first and second capacitor electrodes, and has a thickness less than or equal to 50 Angstroms.

74. (Previously Added): The circuitry of claim 21 wherein the bit lines are received elevationally outward of the memory cell storage capacitors.

75. (Previously Added): The circuitry of claim 28 wherein the bit lines are received elevationally outward of the memory cell storage capacitors.